IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:
Hildebrant
Serial No.: 10/736,438
Filed: 12/15/2003

Confirmation No.: 3423
Group Art Unit: 2112
Examiner: RIZK, Samir Wadie
Docket No. 10030775-1

For: **Systems and Methods for Adaptively Compressing Test Data**

PETITION FOR WITHDRAWAL OF FINAL OFFICE ACTION UNDER 37 C.F.R. §1.181

Mail Stop - Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicant petitions that the final Office Action dated August 07, 2007 (Part of Paper No. 20070731) be withdrawn. Applicant has submitted a statement of facts pursuant to 37 CFR 1.181(b). Submitted as Exhibits in support of the petition and statement of facts is (a) Exhibit A, which includes a copy of the final Office Action dated August 07, 2007, (b) Exhibit B, which includes a copy of Applicant's response to the final Office Action submitted to the USPTO on October 5, 2007, (c) Exhibit C, which includes a copy of the Advisory Action dated October 19, 2007, and (d) Exhibit D, which includes a copy of Applicant's response to the non-final Office Action submitted to the USPTO on June 14, 2007.

As set forth in the statement of facts accompanying the present petition and incorporated herein by reference, Applicant respectfully requests that the final rejection be withdrawn given the confusion in the grounds of rejection and the failure to address explicit claim features (e.g., in the Advisory Action (see (19) and (20) in the statement of facts) and in the final Office Action (when a rejection to one claim is improperly applied to another (see (6) and (7) in the statement of facts)). For instance, the final Office Action (Exhibit A)

provides contradictory explanations as to the grounds of rejection (see statement of facts, (3) – (7)), which was brought to the Examiner's attention in the response to final Office action (Exhibit B) as explained in the statement of facts (see statement of facts (15) – (17)).

The Advisory Action (Exhibit C) failed to address Applicant's request for clarification (see statement of facts, (19)), and makes reference to features (e.g., "clocked pins" as opposed to clock pins and non-clock pins) that do not exist in the pending claims (see statement of facts, (10) – (12) and (19) – (20)).

Applicant further respectfully requests that the Director intervene to address the ambiguity in the final Office Action and Advisory Action as to grounds of rejection and reasoning behind those grounds, and to correct the Examiner's failure to address the explicit claim features.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to deposit account no. 20-0778.

If any further information is required, Applicant requests that the USPTO contact the representative identified below at (770) 933-9500.

Respectfully submitted,

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10/736,438	12/15/2003	Andrew S. Hildebrant	10030775-1	3423

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	PAPER NUMBER
2112	

MAIL DATE	DELIVERY MODE
08/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/736,438	HILDEBRANT ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13,15-17,19-29,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-13,15-17,19-29,31,32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/7/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Response to the applicant's amendment dated 6/14/2007
- Claims 2, 14, 18 and 30 have been Cancelled
- Amended claims 1, 3-13, 15-17, 19-29, 31 and 32 have been submitted for examination
- Amended claims 1, 3-13, 15-17, 19-29, 31 and 32 have been rejected

Response to Arguments

1. Applicant's arguments see pages 8-14, filed on 6/14/2007 have been fully considered but they are not persuasive.

2. The Examiner disagrees with the Applicant assertion in page 9, lines 29-32 that:

"Applicant respectfully submits that there is nothing in this cited section of *Ishida*, nor elsewhere in *Ishida*, that discloses the above-emphasized claim features. Simply monitoring or evaluating data changes does not necessarily involve any determination as to timing complexity. Accordingly, Applicant respectfully submits that claim 1 is allowable over the art of record, and respectfully requests that the rejection be withdrawn. "

The Applicant emphasized the claimed features in amended claim 1:

a) determining a timing complexity for the first plurality of data units;

b) determining a timing complexity for the second plurality of data units;

And, the Applicant goes on to explain that "Simply monitoring or evaluating data changes does not necessarily involve and determination as to timing complexity."

Actually the Applicant has quoted Ishida in page 9, line 22-23 teaches **calculating** a threshold value of the number of data changes. The Examiner maintains that calculating is a means of determining the complexity of the data units as recited in amended claim 1.

3. In regard to claim 14, that is cancelled and the limitation has been incorporated into the independent claim 12, Examiners disagrees with the Applicant quotation of section [0061] in Wang to conclude in page 13, lines 29-31 if the applicant's remarks:

"Neither the above-cited section of *Wang,* nor elsewhere in *Wang,* discloses, teaches, or suggests that the signals pertaining to the external scan input pins 111 and the external primary input pins 113 correspond to clock signals and non-clock signals, respectively."

The Examiner re-iterates that Wang in FIG. 1, reference characters (110) and (113) teaches combinational logic test pins. Combinational logic is inherently non-clock signals to those of ordinary skill in the art. Also, Wang in FIG. 1, reference characters (108), (109) and (111) teaches SC "Scan Chain" test pins. Scan chain is inherently clock signals to those of ordinary skill in the art.

4. The Examiner disagrees with the applicant and maintains the rejection of claims 1, 3-13, 15-17, 19-29, 31 and 32 as in the office action mailed on 3/16/2007. All the amendments and arguments have been considered. It is the Examiner's conclusion that claims 1, 3-13, 15-17, 19-29, 31 and 32 are not patentably distinct or non-obvious over the prior art of record in view of the reference, Ishida and Wang. Therefore the rejection is maintained.

5. The office action rejection mailed on 3/16/2007 copied below in its entirety.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4-7,11,12, 16-18, 20-23, 27, 28 and 32 are rejected under 35

U.S.C. 102(e) as being anticipated by Ishida.

3. In regard to claim 1, Ishida teaches:

examining a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins (col. 2, line 55-56 in Ishida) and a second plurality of data units corresponding to a second plurality of DUT pins (col. 2, line 55-56 in Ishida);
compressing the first plurality of data units using a first compression technique; and compressing the second plurality of data units using a second compression technique (col. 2, lines 57-60 in Ishida).

4. In regard to claim 2, Ishida teaches:

determining a timing complexity for the first plurality of data units; and determining a timing complexity for the second plurality of data units(col. 3, lines 38-47 in Ishida).

5. In regard to claim 4, Ishida teaches:

wherein compressing the first plurality of data units by a predetermined compression rate requires more resources than compressing the second plurality of data units by the predetermined compression rate.
(Note: FIG. 2, in Ishida)

6. In regard to claim 5, Ishida teaches:
wherein the first plurality of data units have a different timing complexity than the second plurality of data units.
(Note; FIG. 6, reference character (65) and col. 3, lines 58-65 in Ishida)

7. In regard to claim 6, Ishida teaches:

wherein the first plurality of data units have a different vector data volume than the second plurality of data units.

(Note: FIG. 1 in Ishida)

8. In regard to claim 7, Ishida teaches:

wherein the first plurality of data units have more repetitive data patterns than the second plurality of data units.

(Note: FIG. 1 in Ishida)

9. In regard to claim 11, Ishida teaches:

wherein at least one processor operating in a first timing domain enables the first plurality of data units to be provided to the first plurality of DUT pins, and at least one processor operating in a second timing domain enables second plurality of data units to be provided to the second plurality of DUT pins, wherein the second timing domain is different from the first timing domain.

(Note; FIG. 112, reference characters (588), (592) & (593) in Ishida)

10. Claim 12 is rejected for the same reasons as per claim 1.

11. Claims 16 and 32 are rejected for the same reasons as per claims 5, 6 and 7.

12. In regard to claim 17, Ishida teaches:

memory configured to store a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins and a second plurality of data units corresponding to a second plurality of DUT pins; and a processor operative to: compress the first plurality of data units using a first compression technique; and compress the second plurality of data units using a second compression technique.

(Note: Figures (112) and (113) in Ishida)

13. Claim 18 is rejected for the same reasons as per claim 2.

14. Claim 20 is rejected for the same reasons as per claim 4.

15. Claim 21 is rejected for the same reasons as per claim 5.

16. Claim 22 is rejected for the same reasons as per claim 6.

17. Claim 23 is rejected for the same reasons as per claim 7.

18. Claim 27 is rejected for the same reasons as per claim 11.

19. Claim 28 is rejected for the same reasons as per claim 17.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

20. Claims 3, 8, 9, 13,14, 19, 24, 25, 29 and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida as applied to claim 1 above, and further in view of Wang et al. US publication no. 2006/0242502 (Hereinafter Wang).

21. In regard to claim 3, Ishida substantially teaches all the limitations in claim 1.

However, Ishida does not teach:

wherein the first plurality of data units corresponds to clock signals and the second plurality of data units corresponds to non-clock signals.

Wang in an analogous art that teaches method and apparatus for broadcasting SCAN patterns in a random access SCAN based integrated circuit teaches:

wherein the first plurality of data units corresponds to clock signals (FIG. 1, reference character (111) in Wang) and the second plurality of data units corresponds to non-clock signals (FIG. 1, reference character (113) in Wang).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Ishida that comprise comprising of test data files with the teaching of Wang.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to cover more faults per scan test pattern.

22. In regard to claim 8, Wang teaches:

wherein the first plurality of DUT pins are clock-pins (FIG. 1, reference character (111) in Wang) and the second plurality of DUT pins are non-clock-pins (FIG. 1, reference character (113) in Wang).

23. In regard to claim 9, Wang teaches:

formatting the first plurality of data units independently from the second plurality of data units.
(Note: FIG. 6 in Wang)

24. Claims 13 and 25 and 29 are rejected for the same reasons as per claim 9.

25. Claim 14 is rejected for the same reasons as per claim 3.

26. Claim 19 is rejected for the same reasons as per claim 3.

27. Claims 24 and 30 are rejected for the same reasons as per claim 8.

28. Claims 10, 15, 26 and 31are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida as applied to claim 1 above, and further in view of Testa et al. US patent no. 6205407 (Hereinafter Testa).

29. In regard to claim 10, Ishida substantially teaches all the limitations in claim 1.

However Ishida does not teach:

wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

Testa in an analogous art that teaches system and method for generating test program codes teaches:

wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file. (Note: col. 9, lines 5-35 in Testa)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Ishida that comprise comprising of test data files with the teaching of Testa.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to cover more faults per scan test pattern.

30. Claims 15, 26, 31 are rejected for the same reasons as per claim 10.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk,

Examiner

ART UNIT 2112

8/2/07

JACQUES LOUIS-JACQUES
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:
Hildebrant
Serial No.: 10/736,438
Filed: 12/15/2003

Confirmation No.: 3423
Group Art Unit: 2112
Examiner: RIZK, Samir Wadie
Docket No. 10030775-1

For: **Systems and Methods for Adaptively Compressing Test Data**

RESPONSE TO FINAL OFFICE ACTION

Mail Stop - AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

The final Office Action mailed August 07, 2007 (Part of Paper No. 20070731) has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

AUTHORIZATION TO DEBIT ACCOUNT

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to deposit account no. 20-0778.

AMENDMENTS

Please amend the present application as follows:

Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("~~---~~"), as is applicable:

1 - 11. (Canceled)

12. (Previously Presented) A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:

examining a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins;

determining that the first plurality of data units have a first compressibility characteristic; and

determining that the second plurality of data units have a second compressibility characteristic.

13. (Original) The method of claim 12, further comprising the step of: compressing the first plurality of data units independently from the second plurality of data units.

14. (Canceled)

15. (Original) The method of claim 12, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

16. (Original) The method of claim 12, wherein the first plurality of data units have a different timing complexity, a different vector data volume, and more repetitive data patterns than the second plurality of data units.

17 - 27. (Canceled)

28. (Previously Presented) A system for adaptively compressing test data to be provided to a device under test (DUT), the system comprising:

memory configured to store a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins; and

a processor that is operative to:

determine that the first plurality of data units have a first compressibility characteristic;

determine that the second plurality of data units have a second compressibility characteristic.

29. (Original) The system of claim 28, wherein the processor is operative to:

compress the first plurality of data units independently from the second plurality of data units.

30. (Canceled)

31. (Original) The system of claim 28, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

32. (Original) The system of claim 28, wherein the first plurality of data units have a different timing complexity, a different vector data volume, and more repetitive data patterns than the second plurality of data unit

REMARKS

This is a full and timely response to the outstanding final Office Action mailed August 07, 2007. Through this response, claims 1, 3-11, 17, and 19-27 have been cancelled without prejudice, waiver, or disclaimer. Reconsideration and allowance of the application and pending claims 12, 13, 15, 16, 28, 29, 31, and 32 are respectfully requested.

I. Claim Rejections - 35 U.S.C. § 102(e)

A. Statement of the Rejection

Claims 1, 2, 4-7, 11, 12, 16-18, 20-23, 27, 28, and 32 have been rejected under 35 U.S.C. § 102(e) as allegedly anticipated by *Ishida et al.* ("*Ishida*," U.S. Pat. No. 6,661,839). Applicant respectfully traverses this rejection where not rendered moot by cancellation of the claims.

Applicant respectfully notes that the final Office action is confusing in that page 5 asserts that claim 12 "is rejected for the same reasons as per claim 1." Similarly, the final Office Action on page 6 alleges that claim 28 "is rejected for the same reasons as claim 17." However, Applicant respectfully notes that claims 1 and 17 lack the below-emphasized features found in claims 12 and 28, respectively, and that those emphasized features are not addressed in the rejection to claims 1 and 17.

Additionally, the confusion is perpetuated by the fact that the "Response to Arguments" section on page 3 appears to attempt to address the arguments presented in support of patentability of claims 12 and 28 in Applicant's last response, but uses *Wang* and fails to address the explicit claim features. Accordingly, Applicant queries whether the rejection to claims 12 and 28 is based on 103(a) (*Ishida* and *Wang*), 102(e) (*Wang*), or 102(e) (*Ishida*). Further, Applicant respectfully submits that the failure to address the explicit claim features renders the rejection improper under MPEP 706 (e.g., 37 CFR 1.104),

and hence Applicant respectfully requests that the next Office Action, if not a Notice of Allowance, be made non-final to accord Applicant an adequate opportunity to address any rejection of the explicit claim features and clarify issues for appeal.

Applicant will assume for purposes of advancing prosecution on the merits that the rejection of the below emphasized claim features is to be addressed under 35 U.S.C. 103(a), and hence the rejection under 102(e) will briefly point out the deficiencies of *Ishida*.

B. Discussion of the Rejection

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102(e).

In the present case, not every claimed feature is represented in the *Ishida* reference. Applicant discusses the *Ishida* reference and Applicant's claims in the following.

Independent Claim 12

Claim 12 recites (with emphasis added):

> 12. A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:
> examining a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, ***wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins***;
> determining that the first plurality of data units have a first compressibility characteristic; and
> determining that the second plurality of data units have a second compressibility characteristic.

Applicant respectfully submits that *Ishida* fails to disclose, teach, or suggest at least the above emphasized claim features. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

Because independent claim 12 is allowable over *Ishida*, dependent claim 16 is allowable as a matter of law for at least the reason that the dependent claim 16 contains all elements of it's respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Independent Claim 28

Claim 28 recites (with emphasis added):

> 28. A system for adaptively compressing test data to be provided to a device under test (DUT), the system comprising:
> memory configured to store a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, ***wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins***; and
> a processor that is operative to:
> determine that the first plurality of data units have a first compressibility characteristic;
> determine that the second plurality of data units have a second compressibility characteristic.

Applicant respectfully submits that *Ishida* fails to disclose, teach, or suggest at least the above emphasized claim features. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

Because independent claim 28 is allowable over *Ishida*, dependent claim 32 is allowable as a matter of law.

Due to the shortcomings of the *Ishida* reference described in the foregoing, Applicant respectfully asserts that *Ishida* does not anticipate Applicant's claims. Therefore, Applicant respectfully requests that the rejection of these claims be withdrawn.

II. Claim Rejections - 35 U.S.C. § 103(a)

A. Statement of the Rejection

Claims 3, 8, 9, 13, 14, 19, 24, 25, 29 and 30 have been rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Ishida* and further in view of *Wang et al.* ("*Wang*," U.S. Publication No. 2006/0242502). Claims 10, 15, 26 and 31 have been rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Ishida* and further in view of *Testa et al.* ("*Testa*," U.S. Pat. No. 6205407). Applicant respectfully traverses these rejections where not rendered moot by cancellation of the claims.

B. Discussion of the Rejection

The U.S. Patent and Trademark Office ("USPTO") has the burden under section 103 to establish a *prima facie* case of obviousness according to the factual inquiries expressed in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). The four factual inquires, also expressed in MPEP 2100-116, are as follows:

(A) Determining the scope and contents of the prior art;

(B) Ascertaining the differences between the prior art and the claims in issue;

(C) Resolving the level of ordinary skill in the pertinent art; and

(D) Evaluating evidence of secondary considerations.

Applicant respectfully submits that a *prima facie* case of obviousness is not established using the art of record.

Claim 12

As set forth above, Applicant respectfully submits that claim 12 is allowable over *Ishida*. The final Office Action alleges the following on page 3 (no emphasis added):

> The Examiner re-iterates that Wang in FIG. 1, reference characters (110) and (113) teaches combinational logic test pins. Combinational logic is inherently non-clock signals to those of ordinary skill in the art. Also, Wang in FIG 1, reference characters (108), (109) and (111) teaches SC "Scan

> Chain" test pins. Scan chain is inherently clock signals to those of ordinary skill in the art.

Applicant respectfully disagrees. Even assuming *arguendo Wang* teaches scan chains, *Wang* does not disclose that the test pins 108, 109 and 111 are ***clock pins***. Indeed, Applicant has reviewed several technical articles (e.g., http://www.ics.uci.edu/~nodari/vts2003.pdf, http://www.caip.rutgers.edu/~bushnell/dsdwebsite/dsdlecture26.ppt, http://www.jtag.com/main.php?cm=p8_1___) and has found no evidence to support the Examiner's conclusion that a "scan chain is inherently clock signals." Quite the contrary, the inputs to the scan chains described and shown in the articles referenced above appear to be non-clock signals.

Further, even assuming *arguendo* evidence can be presented to support clock signal inputs to a scan chain, that evidence alone (in view of other literature such as disclosed above) cannot support an inherency argument since, as set forth in a recent Federal Circuit court decision:

> "[A]nticipation by inherent disclosure is appropriate only when the reference discloses prior art that must necessarily include the unstated limitation." *Atofina v. Great Lakes Chemical Corp.*, 441 F.3d 991, 1000 (Fed. Cir. 2006).

Additionally, Applicant respectfully notes that the explicit claim features are to ***clock-pins***, not clocked pins. Accordingly, Applicant respectfully requests that the rejection to claim 12 be withdrawn.

Claim 28

For similar reasons set forth in association with claim 12, Applicant respectfully submits that *Wang* and *Ishida* fail to disclose, teach, or suggest at least the features emphasized above for claim 28. Accordingly, Applicant respectfully requests that the rejection to claim 28 be withdrawn.

Claims 13 and 29

Applicant respectfully submits that *Ishida* fails to disclose, teach, or suggest at least the above-emphasized features of independent claims 12 and 28. Further, Applicant respectfully submits that *Wang* fails to remedy these deficiencies. For at least the reason that *Ishida* and *Wang* fail to disclose, teach, or suggest at least the features emphasized above for independent claims 12 and 28, dependent claims 13 and 29 (which incorporate the respective allowable base claim features) are allowable as a matter of law. Accordingly, Applicant respectfully requests that the rejection to claims 13 and 29 be withdrawn.

Claims 15 and 31

Applicant respectfully submits that *Ishida* fails to disclose, teach, or suggest at least the above-emphasized features of independent claims 12 and 28. Further, Applicant respectfully submits that *Testa* fails to remedy these deficiencies. For at least the reason that *Ishida* and *Testa* fail to disclose, teach, or suggest at least the features emphasized above for independent claims 12 and 28, dependent claims 15 and 31 (which incorporate the respective allowable base claim features) are allowable as a matter of law. Accordingly, Applicant respectfully requests that the rejection to claims 15 and 31 be withdrawn.

In summary, it is Applicant's position that a *prima facie* for obviousness has not been made against Applicant's claims. Therefore, it is respectfully submitted that each of these claims is patentable over the art of record and that the rejection of these claims should be withdrawn.

III. Canceled Claims

As identified above, claims 1, 3-11, 17, and 19-27 have been canceled from the application through this response without prejudice, waiver, or disclaimer. Applicant reserves the right to present these canceled claims, or variants thereof, in continuing applications to be filed subsequently.

CONCLUSION

Applicant respectfully submit that Applicant's pending claims are in condition for allowance. Any other statements in the Office Action that are not explicitly addressed herein are not intended to be admitted. In addition, any and all findings of inherency are traversed as not having been shown to be necessarily present. Furthermore, any and all findings of well-known art and official notice, and similarly interpreted statements, should not be considered well known since the Office Action does not include specific factual findings predicated on sound technical and scientific reasoning to support such conclusions. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

/dr/
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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,438	12/15/2003	Andrew S. Hildebrant	10030775-1	3423

63448 7590 10/19/2007

VERIGY
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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	PAPER NUMBER
2112	

MAIL DATE	DELIVERY MODE
10/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/736,438	**Applicant(s)** HILDEBRANT ET AL.
	Examiner Sam Rizk	**Art Unit** 2112

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 05 October 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 12,13,15,16,28,29,31,32.
   Claim(s) withdrawn from consideration: ~~1-3,11,17 and 19-27~~.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

JACQUES LOUIS-JACQUES
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Continuation of 11. does NOT place the application in condition for allowance because:

1. Applicant areguments in regard to claims 12 and 28 does not overcome the final rejection. The Examiner maintains that Wang teaches CLOCKED PINS as per the claims 12 and 28 language.

2. The Applicant is refered to section [0029] of the instant application and the disclosure of Wang in FIG. 1, reference characters (108) and (109) of CLOCKED PINS discosure as in claims 12 and 28.

3. Claims amendemnts will be entered.

10/15/07

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Hildebrant

Serial No.: 10/736,438

Filed: 12/15/2003

Confirmation No.: 3423

Group Art Unit: 2112

Examiner: RIZK, Samir Wadie

Docket No. 10030775-1

For: **Systems and Methods for Adaptively Compressing Test Data**

Amendment to be entered
SWR
10/15/07

RESPONSE TO FINAL OFFICE ACTION

Mail Stop - AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

The final Office Action mailed August 07, 2007 (Part of Paper No. 20070731) has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

AUTHORIZATION TO DEBIT ACCOUNT

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to deposit account no. 20-0778.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Hildebrant

Serial No.: 10/736,438

Filed: 12/15/2003

Confirmation No.: 3423

Group Art Unit: 2133

Examiner: RIZK, Samir Wadie

Docket No. 10030775-1

For: **Systems and Methods for Adaptively Compressing Test Data**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

The non-final Office Action mailed March 16, 2007 (Part of Paper No. 20070307) has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

AUTHORIZATION TO DEBIT ACCOUNT

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to deposit account no. 20-0778.

AMENDMENTS

Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("——"), as is applicable:

1. (Currently amended) A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:

examining a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins and a second plurality of data units corresponding to a second plurality of DUT pins;

determining a timing complexity for the first plurality of data units;

determining a timing complexity for the second plurality of data units;

compressing the first plurality of data units using a first compression technique; and

compressing the second plurality of data units using a second compression technique.

2. (Canceled)

3. (Original) The method of claim 1, wherein the first plurality of data units corresponds to clock signals and the second plurality of data units corresponds to non-clock signals.

4. (Original) The method of claim 1, wherein compressing the first plurality of data units by a predetermined compression rate requires more resources than compressing the second plurality of data units by the predetermined compression rate.

5. (Original) The method of claim 1, wherein the first plurality of data units have a different timing complexity than the second plurality of data units.

6. (Original) The method of claim 1, wherein the first plurality of data units have a different vector data volume than the second plurality of data units.

7. (Original) The method of claim 1, wherein the first plurality of data units have more repetitive data patterns than the second plurality of data units.

8. (Original) The method of claim 1, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins.

9. (Original) The method of claim 1, further comprising the step of:

formatting the first plurality of data units independently from the second plurality of data units.

10. (Original) The method of claim 1, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

11. (Original) The method of claim 1, wherein at least one processor operating in a first timing domain enables the first plurality of data units to be provided to the first plurality of DUT pins, and at least one processor operating in a second timing domain enables second plurality of data units to be provided to the second plurality of DUT pins, wherein the second timing domain is different from the first timing domain.

12. (Currently amended) A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:

examining a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins;

determining that the first plurality of data units have a first compressibility characteristic; and

determining that the second plurality of data units have a second compressibility characteristic.

13. (Original) The method of claim 12, further comprising the step of: compressing the first plurality of data units independently from the second plurality of data units.

14. (Canceled)

15. (Original) The method of claim 12, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

16. (Original) The method of claim 12, wherein the first plurality of data units have a different timing complexity, a different vector data volume, and more repetitive data patterns than the second plurality of data units.

17. (Currently amended) A system for adaptively compressing test data to be provided to a device under test (DUT), the system comprising:

memory configured to store a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins and a second plurality of data units corresponding to a second plurality of DUT pins; and

a processor operative to:

determine a timing complexity for the first plurality of data units;

determine a timing complexity for the second plurality of data units;

compress the first plurality of data units using a first compression technique; and

compress the second plurality of data units using a second compression technique.

18. (Canceled)

19. (Original) The system of claim 17, wherein the first plurality of data units correspond to clock signals and the second plurality of data units correspond to non-clock signals.

20. (Original) The system of claim 17, wherein compressing the first plurality of data units by a predetermined compression rate requires more resources than compressing the second plurality of data units by the predetermined compression rate.

21. (Original) The system of claim 17, wherein the first plurality of data units have a different timing complexity than the second plurality of data units.

22. (Original) The system of claim 17, wherein the first plurality of data units have a different vector data volume than the second plurality of data units.

23. (Original) The system of claim 17, wherein the first plurality of data units have more repetitive data patterns than the second plurality of data units.

24. (Original) The system of claim 17, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins.

25. (Original) The system of claim 17, further comprising the step of:

formatting the first plurality of data units independently from the second plurality of data units.

26. (Original) The system of claim 17, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

27. (Original) The system of claim 17, wherein at least one processor operating in a first timing domain enables the first plurality of data units to be provided to the first plurality of DUT pins, and at least one processor operating in a second timing domain enables the second plurality of data units to be provided to the second plurality of DUT pins, wherein the second timing domain is different from the first timing domain.

28. (Currently amended) A system for adaptively compressing test data to be provided to a device under test (DUT), the system comprising:

memory configured to store a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins; and

a processor that is operative to:

determine that the first plurality of data units have a first compressibility characteristic;

determine that the second plurality of data units have a second compressibility characteristic.

29. (Original) The system of claim 28, wherein the processor is operative to:

compress the first plurality of data units independently from the second plurality of data units.

30. (Canceled)

31. (Original) The system of claim 28, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

32. (Original) The system of claim 28, wherein the first plurality of data units have a different timing complexity, a different vector data volume, and more repetitive data patterns than the second plurality of data unit

REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed March 16, 2007. Through this response, independent claims 1, 12, 17, and 28 have been amended, and claims 2, 14, 18, and 30 have been canceled without prejudice, waiver, or disclaimer. Reconsideration and allowance of the application and pending claims 1, 3-13, 15-17, 19-29, and 31-32 are respectfully requested.

I. Claim Rejections - 35 U.S.C. § 102(e)

A. Statement of the Rejection

Claims 1, 2, 4-7, 11, 12, 16-18, 20-23, 27, 28, and 32 have been rejected under 35 U.S.C. § 102(e) as allegedly anticipated by *Ishida et al.* ("*Ishida*," U.S. Pat. No. 6,661,839). Applicant respectfully submits that the amendments to claims 1, 12, 17, and 28 have rendered the rejection moot, and further that claims 1, 2, 4-7, 11, 12, 16-18, 20-23, 27, 28, and 32 are allowable over the art of record.

B. Discussion of the Rejection

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102(e).

In the present case, not every claimed feature is represented in the *Ishida* reference. Applicant discusses the *Ishida* reference and Applicant's claims in the following.

Independent Claim 1

Claim 1 recites (with emphasis added):

> 1. A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:
> examining a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins and a second plurality of data units corresponding to a second plurality of DUT pins;
> ***determining a timing complexity for the first plurality of data units;***
> ***determining a timing complexity for the second plurality of data units***;
> compressing the first plurality of data units using a first compression technique; and
> compressing the second plurality of data units using a second compression technique.

As indicated above, Applicant respectfully submits that the rejection to claim 1 has been rendered moot through amendment. Additionally, Applicant respectfully submits that claim 1 is allowable over *Ishida*. Applicant has amended claim 1 to incorporate features of claim 2, and hence addresses the rejection to claim 2 in the context of amended claim 1. In particular, the Office Action (page 3) refers the Applicant to col. 3, lines 38-47 for support of the rejection of claim 2. That cited section of *Ishida* provides as follows:

> In a datacompressing method of a preferred embodiment, the dividing step includes the steps of: calculating a threshold value of the number of data changes for dividing the input data into unit data sequences; counting the number of data changes of each the divided unit data sequence of the input data; comparing the actual number of data changes with the threshold value; and distributing a divided unit data sequence to one of the plurality of blocks in accordance with the comparison result; whereby the input data can be divided into proper blocks.

Applicant respectfully submits that there is nothing in this cited section of *Ishida*, nor elsewhere in *Ishida*, that discloses the above-emphasized claim features. Simply monitoring or evaluating data changes does not necessarily involve any determination as to timing complexity. Accordingly, Applicant respectfully submits that claim 1 is allowable over the art of record, and respectfully requests that the rejection be withdrawn.

Because independent claim 1 is allowable over *Ishida*, dependent claims 4-7 and 11 are allowable as a matter of law for at least the reason that the dependent claims 4-7 and 11 contain all elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Independent Claim 12

Claim 12 recites (with emphasis added):

> 12. A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:
> examining a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, ***wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins***;
> determining that the first plurality of data units have a first compressibility characteristic; and
> determining that the second plurality of data units have a second compressibility characteristic.

As indicated above, Applicant respectfully submits that the rejection to claim 12 has been rendered moot through amendment. Additionally, Applicant respectfully submits that claim 12 is allowable over *Ishida* and in general, the art of record. Applicant has amended claim 12 to incorporate features of claim 14, but will address the rejection to claim 14 in Section II below. Accordingly, Applicant respectfully submits that claim 12 is allowable over the art of record, and respectfully requests that the rejection be withdrawn.

Because independent claim 12 is allowable over *Ishida*, dependent claim 16 is allowable as a matter of law for at least the reason that the dependent claim 16 contains all elements of it's respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Independent Claim 17

Claim 17 recites (with emphasis added):

> 17. A system for adaptively compressing test data to be provided to a device under test (DUT), the system comprising:
> memory configured to store a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins and a second plurality of data units corresponding to a second plurality of DUT pins; and
> ***a processor operative to:***
> ***determine a timing complexity for the first plurality of data units;***
> ***determine a timing complexity for the second plurality of data units;***
> compress the first plurality of data units using a first compression technique; and
> compress the second plurality of data units using a second compression technique.

As indicated above, Applicant respectfully submits that the rejection to claim 17 has been rendered moot through amendment. Additionally, for similar reasons presented in association with claim 1, Applicant respectfully submits that claim 17 is allowable over *Ishida*, and hence respectfully requests that the rejection to claim 17 be withdrawn.

Because independent claim 17 is allowable over *Ishida*, dependent claims 20-23 and 27 are allowable as a matter of law.

Independent Claim 28

Claim 28 recites (with emphasis added):

> 28. A system for adaptively compressing test data to be provided to a device under test (DUT), the system comprising:
> memory configured to store a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, ***wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins***; and
> a processor that is operative to:
> determine that the first plurality of data units have a first compressibility characteristic;
> determine that the second plurality of data units have a second compressibility characteristic.

As indicated above, Applicant respectfully submits that the rejection to claim 28 has been rendered moot through amendment. Additionally, Applicant respectfully submits that claim 28 is allowable over *Ishida* and in general, the art of record. Applicant has amended claim 28 to incorporate features of claim 30, but will address the rejection to claim 30 in Section II below. Accordingly, Applicant respectfully submits that claim 28 is allowable over the art of record, and respectfully requests that the rejection be withdrawn.

Because independent claim 28 is allowable over *Ishida*, dependent claim 32 is allowable as a matter of law.

Due to the shortcomings of the *Ishida* reference described in the foregoing, Applicant respectfully asserts that *Ishida* does not anticipate Applicant's claims. Therefore, Applicant respectfully requests that the rejection of these claims be withdrawn.

II. Claim Rejections - 35 U.S.C. § 103(a)

A. Statement of the Rejection

Claims 3, 8, 9, 13, 14, 19, 24, 25, 29 and 30 have been rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Ishida* and further in view of *Wang et al.* ("*Wang*," U.S. Publication No. 2006/0242502). Claims 10, 15, 26 and 31 have been rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Ishida* and further in view of *Testa et al.* ("*Testa*," U.S. Pat. No. 6205407). Applicant respectfully traverses these rejections where not rendered moot by amendment.

B. Discussion of the Rejection

The U.S. Patent and Trademark Office ("USPTO") has the burden under section 103 to establish a *prima facie* case of obviousness according to the factual inquiries expressed in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). The four factual inquires, also expressed in MPEP 2100-116, are as follows:

(A) Determining the scope and contents of the prior art;

(B) Ascertaining the differences between the prior art and the claims in issue;

(C) Resolving the level of ordinary skill in the pertinent art; and

(D) Evaluating evidence of secondary considerations.

Applicant respectfully submits that a *prima facie* case of obviousness is not established using the art of record.

Claims 3, 8, 9, 13, 14, 19, 24, 25, 29, and 30

Applicant respectfully submits that *Ishida* fails to disclose, teach, or suggest at least the above-emphasized features of independent claims 1, 12, 17, and 28. Further, Applicant respectfully submits that *Wang* fails to remedy these deficiencies. For instance, with regard to claim 14, the features of which are incorporated into independent claim 12, the Office Action refers to the rejection of claim 3 for an explanation as to the reasons for the rejection. The Office Action addresses the reasoning for the rejection of claim 3 on pages 5 and 6 by referencing Figure 1 of *Wang*, and in particular reference characters 111 (allegedly for clock signals) and 113 (allegedly for non-clock signals). In the description of *Wang* corresponding to reference characters 111 and 113, *Wang* provides as follows in paragraph [0061]:

> [0061] The ATE 102 applies a set of fully specified test patterns 103, one by one, to the CUT 107 via scan chains 109 in scan mode from external scan input pins 111 as well as from external primary input pins 113. The CUT is then run in normal mode using the applied test pattern as input, and the response to the test pattern is captured into the scan chains. The CUT is then put back into scan mode again and the test response is shifted out to the ATE via scan chains from external scan output pins 112 as well as from external primary output pins 114. The shifted-out test response 104 is then compared by the comparator 105 with the corresponding expected test response 106 to determine if any fault exists in the CUT, and indicates the result by the pass/fail signal 115.

Neither the above-cited section of *Wang*, nor elsewhere in *Wang*, discloses, teaches, or suggests that the signals pertaining to the external scan input pins 111 and the external primary input pins 113 correspond to clock signals and non-clock signals, respectively. As

another example, and for similar reasons explained in association with claim 14, the rejection to claim 30 (features of which are incorporated into independent claim 28) fails to disclose, teach, or suggest at least the features emphasized above in amended independent claim 28. For at least the reason that *Ishida* and *Wang* fail to disclose, teach, or suggest at least the features emphasized above for independent claims 1, 12, 17, and 28, dependent claims 3, 8, 9, 13, 14, 19, 24, 25, 29, and 30 (which incorporate the respective allowable base claim features) are allowable as a matter of law. Accordingly, Applicant respectfully requests that the rejection to claims 3, 8, 9, 13, 14, 19, 24, 25, 29, and 30 be withdrawn.

Claims 10, 15, 26, and 31

Applicant respectfully submits that *Ishida* fails to disclose, teach, or suggest at least the above-emphasized features of independent claims 1, 12, 17, and 28. Further, Applicant respectfully submits that *Testa* fails to remedy these deficiencies. For at least the reason that *Ishida* and *Testa* fail to disclose, teach, or suggest at least the features emphasized above for independent claims 1, 12, 17, and 28, dependent claims 10, 15, 26, and 31 (which incorporate the respective allowable base claim features) are allowable as a matter of law. Accordingly, Applicant respectfully requests that the rejection to claims 10, 15, 26, and 31 be withdrawn.

In summary, it is Applicant's position that a *prima facie* for obviousness has not been made against Applicant's claims. Therefore, it is respectfully submitted that each of these claims is patentable over the art of record and that the rejection of these claims should be withdrawn.

III. Canceled Claims

As identified above, claims 2, 14, 18, and 30 have been canceled from the application through this Response without prejudice, waiver, or disclaimer. Applicant

reserves the right to present these canceled claims, or variants thereof, in continuing applications to be filed subsequently.

CONCLUSION

Applicant respectfully submit that Applicant's pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. Any other statements in the Office Action that are not explicitly addressed herein are not intended to be admitted. In addition, any and all findings of inherency are traversed as not having been shown to be necessarily present. Furthermore, any and all findings of well-known art and official notice, and similarly interpreted statements, should not be considered well known since the Office Action does not include specific factual findings predicated on sound technical and scientific reasoning to support such conclusions. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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